CLAIMS

What is claimed is:

1. A memory module for an embedded PC system, the memory module comprising:

a NAND interface device adapted to be coupled to a first chip select of a dedicated SDRAM bus; and

at least one NAND memory device coupled to the NAND interface device, wherein the first chip select is utilized to access the NAND memory device via the NAND interface device, and wherein the NAND interface device and the at least one NAND memory device function substantially as a hard disk in the embedded PC system.

2. The memory module of claim 1 further comprising at least one synchronous dynamic random access memory (SDRAM) device adapted to be coupled to a second chip select of the dedicated SDRAM bus, wherein the second chip select is utilized to access the at least one SDRAM device.

3. The memory module of claim 2 wherein the at least one SDRAM device is coupled to a first side of the memory module and wherein the at least one NAND memory device is coupled to a second side of the memory module.

4. The memory module of claim 2 wherein the at least one SDRAM device and the NAND interface device can be adapted to be soldered directly to the dedicated

SDRAM bus, and wherein the at least one NAND memory device can be adapted to be soldered directly to the NAND interface device.

5. The memory module of claim 1 wherein the NAND interface device can be adapted to be soldered directly to the dedicated SDRAM bus, and wherein the at least one NAND memory device can be adapted to be soldered directly to the NAND interface device.

6. The memory module of claim 1 wherein the memory module is adapted to be coupled to a dual inline memory module (DIMM) slot.

7. The memory module of claim 1 wherein the memory module is a dual inline memory module (DIMM).

8. An embedded PC system comprising:

a processor;

a dedicated SDRAM bus coupled to the processor; and

a memory module coupled to the SDRAM bus, the memory module comprising:

a NAND interface device adapted to be coupled to a first chip select of the dedicated SDRAM bus; and

at least one NAND memory device coupled to the NAND interface device, wherein the first chip select is utilized to access the NAND memory device via the NAND interface device, and wherein the NAND interface device and the at least one NAND memory device function substantially as a hard disk in the embedded PC system.

9. The memory module of claim 8 further comprising at least one synchronous dynamic random access memory (SDRAM) device adapted to be coupled to a second chip select of the dedicated SDRAM bus, wherein the second chip select is utilized to access the at least one SDRAM device.

10. The memory module of claim 9 wherein the at least one SDRAM device is coupled to a first side of the memory module and wherein the at least one NAND memory device is coupled to a second side of the memory module.

11. The memory module of claim 9 wherein the at least one SDRAM device and the NAND interface device can be adapted to be soldered directly to the dedicated SDRAM bus, and wherein the at least one NAND memory device can be adapted to be soldered directly to the NAND interface device.

12. The system of claim 8 wherein the NAND interface device can be adapted to be soldered directly to the dedicated SDRAM bus, and wherein the at least one NAND memory device can be adapted to be soldered directly to the NAND interface device.

13. The system of claim 8 wherein the memory module is adapted to be coupled to a dual inline memory module (DIMM) slot.

14. The system of claim 8 wherein the memory module is a dual inline memory module (DIMM).

15. A method for implementing a NAND memory interface, the method comprising:

(a) coupling a first chip select to a NAND interface device, wherein the first chip select is from a dedicated SDRAM bus;

(b) coupling at least one NAND memory device to the NAND interface device; and

(c) utilizing the first chip select to access the at least one NAND memory device via the NAND interface device, wherein the NAND interface device and the at least one NAND memory device function substantially as a hard disk in the embedded PC system.

16. The method of claim 15 wherein the first chip select coupling step (a) comprises the step of (a1) soldering the NAND interface device directly to the dedicated SDRAM bus.

17. The method of claim 16 wherein the at least one NAND memory device coupling step (b) comprises the step of (b1) soldering the at least one NAND memory device directly to the NAND interface device.

18. The method of claim 15 further comprising:

(d) coupling a second chip select to at least one SDRAM device, wherein the second chip select is from the dedicated SDRAM bus; and

(e) utilizing the second chip select to access the at least one SDRAM device.

19. The method of claim 18 further comprising:

(f) coupling the at least one SDRAM device to a first side of a memory module; and

(g) coupling the at least one NAND memory device to a second side of the memory module.

20. The memory module of claim 19 wherein the memory module is a dual inline memory module (DIMM).

21. The method of claim 18 wherein the second chip select coupling step (d) comprises the step of (d1) soldering the at least one SDRAM device directly to the dedicated SDRAM bus.

22. A computer-readable medium including program instructions for implementing a NAND memory interface, the program instructions comprising:

(a) coupling a first chip select to a NAND interface device, wherein the first chip select is from a dedicated SDRAM bus;

(b) coupling at least one NAND memory device to the NAND interface device; and

(c) utilizing the first chip select to access the at least one NAND memory device via the NAND interface device, wherein the NAND interface device and the at least one NAND memory device function substantially as a hard disk in the embedded PC system.

23. The computer-readable medium of claim 22 wherein the first chip select coupling step (a) comprises the step of (a1) soldering the NAND interface device directly to the dedicated SDRAM bus.

24. The computer-readable medium of claim 23 wherein at least one NAND memory device coupling step (b) comprises the step of (b1) soldering the at least one NAND memory device directly to the NAND interface device.

25. The computer-readable medium of claim 22 further comprising program instructions for:

(d) coupling a second chip select to at least one SDRAM device, wherein the second chip select is from the dedicated SDRAM bus; and

(e) utilizing the second chip select to access the at least one SDRAM device.

26. The computer-readable medium of claim 25 further comprising program instructions for:

(f) coupling the at least one SDRAM device to a first side of a memory module; and

(g) coupling the at least one NAND memory device to a second side of the memory module.

27. The computer-readable medium of claim 26 wherein the memory module is a dual inline memory module (DIMM).

28. The computer-readable medium of claim 25 wherein the second chip select coupling step (d) comprises the step of (d1) soldering the at least one SDRAM device directly to the dedicated SDRAM bus.